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REMARKS

Claims 1-27 are currently pending in the subject application and are presently under consideration. Claims 1, 13, 17, 18, 21 and 25 have been amended and claim 5 has been cancelled herein. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1-14 and 17-26 Under 35 U.S.C. §102(e)

Claims 1-14 and 17-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Le et al. (US 6,690,602). This rejection should be withdrawn for at least the following reasons. Le et al. fails to disclose or suggest all limitations of the subject claims.

A single prior art reference anticipates a patent claim only if it *expressly or inherently describes each and every limitation set forth in the patent claim*. *Trintec Industries, Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaa Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). *The identical invention must be shown in as complete detail as is contained in the ... claim*. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Applicants' claimed invention relates to a core based multi-bit memory having a dual bit dynamic referencing architecture fabricated on a memory core comprising a plurality of data cells. In particular, independent claims 1, 13, 17 and 24 recite similar features, namely an architecture that facilitates a reference voltage in a multi-bit memory, comprising a multi-bit memory core including a plurality of data cells for storing data; first and second reference arrays of a plurality of multi-bit reference cells fabricated on the memory core, *the plurality of multi-bit reference cells each associated with separate wordlines within the multi-bit memory core; and a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array* to arrive at the reference voltage employed during a data cell read operation. Le et al. is silent regarding such novel aspects of the subject claims.

Le et al. relates to a system having a memory array and an associated reference array. The cited reference provides for a method of monitoring the aging of data cells by comparing the

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value of a cell within the memory core with averaged data from two reference cells within a single reference array. On page 3 of the Office Action, the Examiner incorrectly contends that Figure 4 of *Le et al.* teaches *a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array*, as in the claimed invention. *Le et al.* allows for core memory cells to be compared to an averaged reference cell value, but the reference does not use reference cell values from different arrays. To the contrary, *Le et al.* compares aging analyzes aging characteristics of data cells to an average value derived from a *single* reference array. See col. 4, lines 15–17. Therefore, since *Le et al.* does not utilize *a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array* as in the claimed invention, *Le et al.* does not provide the increased accuracy with respect to the derived reference voltage as afforded by the claimed invention.

Furthermore, it is incorrectly asserted that Figure 4 of *Le et al.* teaches the claimed feature of a plurality of the multi-bit reference pairs associated with and attached to a corresponding wordline. Figure 4 of *Le et al.* illustrates dynamic reference cells A and B associated with an entire sector of cells that includes a plurality of wordlines. Nowhere does the reference teach that the multiple wordlines within a multi-bit memory core are each associated with separate reference pairs. Consequently, *Le et al.* is silent regarding *a plurality of multi-bit reference pairs each associated with separate wordlines within the multi-bit memory core*, as recited in amended independent claims 1, 13, 17 and 24.

In view of at least the foregoing it is readily apparent that *Le et al.* does not teach the identical invention in as complete detail as is contained in the subject claims. Accordingly, this rejection with respect to independent claims 1, 13, 17 and 24 (and the claims that depend from) should be withdrawn.

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II. Rejection of Claims 16 and 27 Under 35 U.S.C. §103(a)

Claims 16 and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Le et al.* in view of *Kurihara et al.* (US 6,791,880). Withdrawal of this rejection is requested for at least the following reasons. As previously discussed, *Le et al.* fails to disclose all limitations of independent claims 13 and 24 (from which claims 16 and 27 depend from). *Kurihara et al.* fails to compensate for the aforementioned deficiencies of *Le et al.* Accordingly, this rejection should be withdrawn.

III. Rejection of Claim 15 Under 35 U.S.C. §103(a)

Claim 15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Le et al.* in view of *Ferrant* (US 6,538,942). Applicants' representative respectfully requests that this rejection be withdrawn for at least the following reasons. As discussed *supra*, *Le et al.* fails to disclose or suggest all features of independent claim 13 (from which claim 15 depends). *Ferrant* fails to make up for the aforementioned deficiencies of *Le et al.* Therefore, applicants' representative respectfully requests that this rejection be withdrawn.

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CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP975US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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